CLAIMS

What is claimed is:

1. A system, comprising:

a memory access logic configured to be operably connected to a main memory and a processor, the memory access logic comprising:

a memory configured to store contents of a main memory location and to accept memory access requests for the main memory location from the processor while the contents of the main memory location are stored in the memory; and

a scrub logic configured to selectively mirror the main memory location into the memory and to selectively scrub the main memory location.

2. The system of claim 1, where the memory access logic comprises an ASIC.

3. The system of claim 1, where the memory access logic comprises a PROM.

4. The system of claim 1, including a second memory configured to store one or more configuration parameters associated with scrubbing the main memory location, and where the scrub logic is further configured to selectively scrub the main memory location based, at least in part, on one or more of the configuration parameters.

5. The system of claim 4, where the second memory comprises one or more registers.

6. The system of claim 4, where the second memory is writeable by an application located external to the memory access logic.

7. The system of claim 4, where the second memory stores one or more of, an on/off parameter, an address of a main memory location to be scrubbed, a starting address of a range of main memory locations to be scrubbed, an ending address of the range of main memory

locations to be scrubbed, a rate parameter associated with the rate at which main memory scrubbing is to occur, and a log configuration parameter.

8. The system of claim 7, where the log configuration parameter stores one or more entry point addresses for one or more logging processes.

9. The system of claim 1, including a log configured to store a result value associated with scrubbing the main memory location, and where the scrub logic is further configured to selectively produce the result value.

10. The system of claim 9, where the log comprises one or more registers.

11. The system of claim 9, where the log is readable by an application located external to the memory access logic.

12. The system of claim 1, where the scrub logic is configured to selectively generate a signal when the main memory location that is being scrubbed exhibits a memory error.

13. The system of claim 1, where the scrub logic is configured to initiate scrubbing the main memory location by sending one or more signals to an onboard memory testing logic, where the onboard memory testing logic is physically connected to the main memory location.

14. The system of claim 1, where the scrub logic is writeable by an application located external to the memory access logic.

15. The system of claim 1, where the scrub logic is configured to scrub the main memory location substantially transparently to operating system control of main memory.

16. The system of claim 1, where the system is embedded in a computer.

17. The system of claim 1, where the system is embedded in an image forming device.

18. A system, comprising:

a memory access logic configured to be operably connected to a main memory and a processor, the memory access logic comprising:

a memory configured to store the contents of a main memory location and to accept memory access requests for the main memory location from the processor while the contents of the main memory location are stored in the memory; and

a fault management logic configured to selectively process a memory fault associated with the main memory location.

19. The system of claim 18, where the memory access logic comprises an ASIC.

20. The system of claim 18 where the memory access logic comprises a PROM.

21. The system of claim 18, including a second memory configured to store one or more configuration parameters associated with the fault management processing of the main memory location, and where the fault management logic is further configured to selectively process the memory fault based, at least in part, on the configuration parameters.

22. The system of claim 21, where the second memory comprises one or more registers.

23. The system of claim 21, where the second memory is writeable by an application located external to the memory access logic.

24. The system of claim 21, where the second memory stores one or more of, an on/off parameter, an address of a main memory location for which fault management processing is to be performed, a starting address of a range of main memory locations for which fault management processing is to be performed, an ending address of the range of main memory locations for which fault management processing is to be performed, a rate parameter associated with the rate at which main memory fault management processing is to occur, and a log configuration parameter.

25. The system of claim 24, where the log configuration parameter stores one or more entry point addresses for one or more fault management processes.

26. The system of claim 18, including a log configured to store a result value associated with fault management processing of a memory fault experienced by the main memory location, and where the fault management logic is further configured to selectively produce the result value.

27. The system of claim 26, where the log comprises one or more registers.

28. The system of claim 26, where the log is readable by an application external to the memory access logic.

29. The system of claim 18, where the fault management logic is configured to selectively generate a signal when the main memory location exhibits a memory fault.

30. The system of claim 18, where the fault management logic is writeable by an application external to the memory access logic.

31. The system of claim 18, where the fault management logic is configured to perform fault management processing for the main memory location substantially transparently to operating system control of main memory.

32. The system of claim 31, where the fault management logic is further configured to perform one or more of, selectively logging data associated with the memory fault, selectively attempting to correct the memory fault, selectively logically removing the main memory location from the main memory, and selectively halting the operation of a computer with which the system is associated.

33. The system of claim 18, where the system is embedded in one or more of a computer and an image forming device.

34. A system, comprising:

a main memory controller configured to be operably connected to a main memory and a processor, the main memory controller comprising:

a memory configured to logically replace one or more main memory locations;

a scrub logic configured to selectively scrub the one or more main memory locations; and

a fault management logic configured to selectively process a memory fault generated by the one or more main memory locations.

35. The system of claim 34, where the main memory controller comprises an ASIC.

36. The system of claim 34, where the main memory controller comprises a PROM.

37. The system of claim 34, including a second memory configured to store one or more configuration parameters associated with scrubbing the one or more main memory locations or processing a memory fault generated by the one or more main memory locations, where the scrub logic is further configured to selectively scrub the main memory locations based, at least in part, on one or more of the configuration parameters, and where the fault management logic is further configured to selectively process a memory fault generated by the main memory locations based, at least in part, on one or more of the configuration parameters.

38. The system of claim 37, where the second memory comprises one or more registers.

39. The system of claim 37, where the second memory is writeable by an application.

40. The system of claim 37, where the second memory stores one or more of, one or more on/off parameters, an address of a main memory location to be scrubbed, a starting address of a range of main memory locations to be scrubbed, an ending address of the range of main memory locations to be scrubbed, a rate parameter associated with the rate at which main memory scrubbing is to occur, an address of a main memory location for which fault management processing is to be performed, a start address of a range of main memory locations for which fault management processing is to be performed, an ending address of the

range of main memory locations for which fault management processing is to be performed, and a log configuration parameter.

41. The system of claim 40, where the log configuration parameter stores one or more entry point addresses for one or more fault management processes.

42. The system of claim 34, including a log configured to store a result value associated with scrubbing the main memory locations or processing a memory fault generated by the main memory locations and where the fault management logic is further configured to selectively produce the result value.

43. The system of claim 42, where the log comprises one or more registers.

44. The system of claim 42, where the log is readable by an application.

45. The system of claim 34, where the scrub logic is further configured to initiate scrubbing the main memory locations by sending one or more signals to an onboard memory testing logic, where the onboard memory testing logic is physically connected to the main memory locations.

46. The system of claim 34, where the scrub logic is writeable by an application.

47. The system of claim 34, where the fault management logic is writeable by an application.

48. The system of claim 34, where the scrub logic is further configured to scrub the main memory locations substantially transparently to operating system control of main memory.

49. The system of claim 34, where the fault management logic is further configured to process memory faults generated by the main memory locations substantially transparently to operating system control of main memory.

50. The system of claim 34, where the system is embedded in a computer.

51. The system of claim 34, where the system is embedded in an image forming device.

52. A method, comprising:

selectively copying contents of a main memory location to a cache memory location in a main memory controller chipset;

logically replacing the main memory location with the cache memory location; and

memory testing the main memory location, where the memory testing is performed by a testing logic in the main memory controller chipset.

53. The method of claim 52, comprising:

selectively processing a memory fault associated with the main memory location when the memory testing of the main memory location produces a memory fault, where the memory fault processing is performed in the main memory controller chipset.

54. The method of claim 53, where the fault management processing includes one or more of, selectively logging data associated with the memory fault, selectively attempting to correct the memory fault, selectively logically removing the main memory location from the main memory, and selectively halting the operation of a system to which the main memory controller chipset is operably connected.

55. The method of claim 52, where the main memory location can be scrubbed or tested by one or more of, writing back corrected data to the memory location, a parity test, an electrical test, a striping test, a marching ones test, a marching zeroes test, and a pattern test.

56. A computer-readable medium storing processor executable instructions operable to perform a method, the method comprising:

selectively copying contents of a main memory location to a cache memory location in a main memory controller chipset;

logically replacing the main memory location with the cache memory location;

memory testing the main memory location, where the memory testing is performed by a testing logic in the main memory controller chipset; and

selectively processing a memory fault associated with the main memory location when the memory testing of the main memory location produces a memory fault, where the fault management processing is performed in the main memory controller chipset.

57. A memory access system, comprising:

a memory access logic configured to be operably connected to a main memory and a processor, the memory access logic including:

a memory;

a logic configured to:

select a memory location from the main memory and copy contents of the memory location to the memory;

cause memory access requests directed to the memory location to be redirected to the memory; and

perform memory management operations for the memory location while the contents of the memory location are accessible through the memory without disturbing the operation of components configured to access the memory location.

58. The memory access system of claim 57, where the memory management operations include memory scrubbing.

59. The memory access system of claim 57, where the memory management operations include fault processing.

60. A method, comprising:

selecting a memory location having data contents;

copying the data contents to an alternative location in a chipset;

in the chipset, performing memory management operations for the memory location while the memory location is accessible to one or more components; and

causing memory requests from the one or more components to be redirected to the alternative location.

61. The method of claim 60, where the memory management operations include memory scrubbing.

62. The method of claim 60, where the memory management operations include fault processing.

63. A system, comprising:

means for logically replacing a main memory location with a cache memory location in a main memory controller chipset, where the means for logically replacing are located in the main memory controller chipset;

means for testing the main memory location, where the means for testing the main memory location are located in the main memory controller chipset; and

means for managing memory faults associated with the main memory location, where the means for managing memory faults are located in the main memory controller chipset.